IN THE SPECIFICATION:

Please replace paragraph [0002] with the following amended paragraph:

[0002] Embodiments of the present invention relate[[s]] generally to a decoder for decoding convolutional codes, and more particularly, to a Viterbi decoder for decoding a convolutional code on the basis of a Radix-2^x trellis ~~as claimed in the preamble of patent claim 1~~.

Please replace paragraph [0078] with the following amended paragraph:

[0078] The object of the invention is to design a Viterbi decoder which operates using bit pipelining, such that it has the capability for higher throughput rates than are possible with the previous prior art. According to the invention, this object [[is]] may be achieved by a first calculation unit for calculating 2^x branch metrics as m-bit words using periodically successive multibit words in an input sequence for each trellis state, a second calculation unit having parallel cascades of processor elements for, in a current clock period, adding the 2^x branch matrics calculated by the first calculation unit to accumulated 2^x path metrics from 2^x predecessor trellis states and a selection device for selecting a subset of the 2^x path metrics for use as accumulated 2^x path metrics in an addition process in a subsequent clock period, wherein the number of processor elements in each of the cascades is less than the number m of the m-bit words and a third calculation unit for storage of information obtained from the second calculation unit relating to the identity of the selected path metrics ~~the features specified in patent claim 1~~.